STAR Trigger DSM Register List

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This table lists all the registers in the all the algorithms that are loaded into the STAR Trigger DSM boards. These registers control the operation of the algorithms: setting thresholds on ADC values, putting windows on TAC values and selecting which bits get used to make the trigger decision.

Object	Index	Register	Name	Default value	Bit mask	Description
1			L1			
	21		CB201	0x7	0x7	Topology Selection Bit 0: veto "out-of-time" hits Bit 1: veto "overflows" Bit 2: use UPC algorithm for topology decision
	23	0	LD301	0x3	0x3	EMC Etot Select (1,2,3)
		1		0x64	0xff	Minimum Bias prescale
		2		0x1f	0xff	FPD1 mask
		3		0xe0	0xff	FPD2 mask
	25	0	VT201	0x0a0	0x1ff	BBC DeltaT Min0
		1		0x160	0x1ff	BBC DeltaT Max0
		2		0x0a0	0x1ff	BBC-DeltaT Min1
		3		0x160	0x1ff	BBC-DeltaT Max1
		4		0x0a0	0x1ff	ZDC-DeltaT Min0
		5		0x160	0x1ff	ZDC-DeltaT Max0
		6		0x0a0	0x1ff	ZDC-DeltaT Min1
		7		0x160	0x1ff	ZDC-DeltaT Max1
		8		0x5	0x7	BBC Small Tile DeltaT Scalar Bit
		9		0x6	0x7	BBC Large Tile DeltaT Scalar Bit
		10		0x5	0x7	ZDC DeltaT Scalar Bit
	26	0	EM201	0	0xff	BEMC Energy Sum Threshold
		1		0	0x3f	EEMC Energy Sum Threshold
		2		0	0x3	Threshold Select J/Ψ (0,1,2)
		3		3	0x3	Barrel Sum East-West select (1,2,3)
		4		0	0xff	BEMC+EEMC Energy Sum Threshold
	27	0	BX201	0	0xffff	BXing start value: 16 LSB
		1		0	0xffff	BXing start value: 16 next bits
		2		1	0xffff	Rev Tick synch enable
	28	0	BX202	0	0xffff	BXing start: 16 MSB
	29	0	ST201	0x6cd8	0xffff	Zero-bias prescale: 16 LSB
		1		1	0xffff	Zero-bias prescale: 16 MSB
		2		0	0xfff	Random rate: 12 LSB
		3		0	0xfff	Random rate: 12 MSB
	30	0	FP201	0x0	0x3fff	FPD East ADC sum low threshold

		1		0x0	0x3fff	FPD East ADC sum med threshold
		2		0x0	0x3fff	FPD East ADC sum high threshold
		3		0x0	0x3fff	FPD++ S3, S4 threshold 0
		4		0x0	0x7fff	FPD++ S13, S24 threshold 0
		5		0x0	0x3fff	FPD++ S1, S2 threshold 0
		6		0x0	0x3fff	FPD++ S3, S4 threshold 1
		7		0x0	0x7fff	FPD++ S13, S24 threshold 1
		8		0x0	0xffff	FPD++ S1234 threshold 0
		9		0x0	0x7fff	FPD East Sum-NE-SE threshold 0
2			BC1			
	33	0	BE101	0	0xfff	BEMC-jet-patch-th0
		1		1	0xfff	BEMC-jet-patch-th1
		2		2	0xfff	BEMC-jet-patch-th2
		3		2	0x3	BEMC-TP-select (1,2,3)
		4		2	0x3	BEMC HT.TP-select (1,2,3)
	16		BE102			same as 33
	17		BE103			same as 33
	18		BW101			same as 33
	19		BW102			same as 33
	20		BW103			same as 33
	21	0	EE101	0	0x7ff	EEMC-jet-patch-th0
		1		1	0x7ff	EEMC-jet-patch-th1
		2		2	0x7ff	EEMC-jet-patch-th2
		3		2	0x3	EEMC-TP-select (1,2,3)
		4		2	0x3	EEMC-HT.TP-select (1,2,3)
	22		EE102			same as 21
	23	0	EE001	0x04	0x3f	EEMC-high-tower-th0
		1		0x09	0x3f	EEMC-high-tower-th1
		2		0x0e	0x3f	EEMC-high-tower-th2
		3		0x04	0x3f	EEMC-trigger-patch-th0
		4		0x09	0x3f	EEMC-trigger-patch-th1
		5		0x0e	0x3f	EEMC-trigger-patch-th2
	24		EE002			same as 23
	25		EE003			same as 23
	26		EE004			same as 23
	27		EE005			same as 23
	28		EE006			same as 23
	29		EE007			same as 23
	30		EE008			same as 23
	31		EE009			same as 23
3			MWC			No registers used
4			CTB			
	16	0	CB001	0x0	0xf	CTB deadtime in RS’s
		1		0x000	0xfff	Min ADC sum for topology alg.
		2		0xfff	0xfff	Max ADC sum for topology alg.
		3		0x0	0xf	Min. slat sun for topology alg.
		4		0xf	0xf	Max. slat sum for topology alg.
	17		CB002			same as 16
	18		CB003			same as 16
	19		CB004			same as 16

	20		CB005			same as 16
	21		CB006			same as 16
	22		CB007			same as 16
	23		CB008			same as 16
	24		CB009			same as 16
	25		CB010			same as 16
	26		CB011			same as 16
	27		CB012			same as 16
	28		CB013			same as 16
	29		CB014			same as 16
	30		CB015			same as 16
	31		CB016			Same as 16
5			BCW			
	16	0	BW001	0	0x3f	BEMC-West high-tower-th0
		1		1	0x3f	BEMC-West high-tower-th1
		2		2	0x3f	BEMC-West high-tower-th2
		3		0	0x3f	BEMC-West trigger-patch-th0
		4		1	0x3f	BEMC-West trigger-patch-th1
		5		2	0x3f	BEMC-West trigger-patch-th2
	17		BW002			same as 16
	18		BW003			same as 16
	19		BW004			same as 16
	20		BW005			same as 16
	21		BW006			same as 16
	22		BW007			same as 16
	23		BW008			same as 16
	24		BW009			same as 16
	25		BW010			same as 16
	26		BW011			same as 16
	27		BW012			same as 16
	28		BW013			same as 16
	29		BW014			same as 16
	30		BW015			same as 16
6			BCE			
	16	0	BE001	0	0x3f	BEMC-East high-tower-th0
		1		1	0x3f	BEMC-East high-tower-th1
		2		2	0x3f	BEMC-East high-tower-th2
		3		0	0x3f	BEMC-East trigger-patch-th0
		4		1	0x3f	BEMC-East trigger-patch-th1
		5		2	0x3f	BEMC-East trigger-patch-th2
	17		BE002			same as 16
	18		BE003			same as 16
	19		BE004			same as 16
	20		BE005			same as 16
	21		BE006			same as 16
	22		BE007			same as 16
	23		BE008			same as 16
	24		BE009			same as 16
	25		BE010			same as 16
	26		BE011			same as 16
	27		BE012			same as 16

	28		BE013			same as 16
	29		BE014			same as 16
	30		BE015			same as 16
7			EEC			This crate no longer exists
8			BBC			
	16	0	BB001	0x4	0xff	BBC small-tile ADC threshold
		1		0x0	0xff	BBC small-tile TAC Min
		2		0xff	0xff	BBC small-tile TAC Max
		3		0x0	0xf	BBC small-tile thr. deadtime in RS's
	18		BB002			same as 16
	20		BB003			same as 16
	22		BB004			same as 16
	24	0	BB005	0x4	0xff	BBC large-tile ADC threshold
		1		0x0	0xff	BBC large-tile TAC Min
		2		0xff	0xff	BBC large-tile TAC Max
		3		0x0	0xf	BBC large-tile thr. deadtime in RS's
	25		BB006			same as 24
	26	0	BB101	0xa	0x7ff	BBCE small-tile ADC th0
		1		0xa	0x7ff	BBCW small-tile ADC th0
		2		0xf	0x7ff	BBCE small-tile ADC th1
		3		0xf	0x7ff	BBCW small-tile ADC th1
	27	0	BB102	0xa	0x7ff	BBCE large-tile ADC th0
		1		0xa	0x7ff	BBCW large-tile ADC th0
		2		0xf	0x7ff	BBCE large-tile ADC th1
		3		0xf	0x7ff	BBCW large-tile ADC th1
	28	0	MD001	0x5	0xff	MTD ADC threshold
	30	0	ZD001	0x5	0xff	ZDCE-ADC-th0
		1		0x5	0xff	ZDCW-ADC-th0
		2		0xf	0xff	ZDCE-ADC-th1
		3		0xf	0xff	ZDCW-ADC-th1
		4		0x0	0xff	ZDCE-TAC-min
		5		0x0	0xff	ZDCW-TAC-min
		6		0xa	0xf	ZDC-th0-deadtime in RS's
		7		0xa	0xf	ZDC-th1-deadtime in RS's
		8		0xa	0xf	ZDC-timewin-deadtime in RS's
		9		0x50	0xff	ZDC-sum-att-th
		10		0x0a	0xf	ZDC-sum-att-deadtime in RS's
		11		0xff	0xff	ZDCE-TAC-max
		12		0xff	0xff	ZDCW-TAC-max
9			FPE			
	23	0	FE101	0xff	0xff	FPE Module bitmask 1 (8 bits)
	28	0	FE102	0xf	0xf	FPE Module bitmask 2 (4 bits)
10			FPW			
	23	0	FW101	0xff	0xff	FPD++ Module bitmask 1 (8 bits)
	28	0	FW102	0xf	0xf	FPD++ Module bitmask 2 (4 bits)

Change Log:

11th January 2005:

Object 1, Index 30, FP201:

Changed “FPD ADC sum low threshold” to “FPD East ADC sum low threshold”
Same for “med” and “high” thresholds.
Changed “Threshold select” to “High-Tower Threshold select”. This register is no longer used by the Sum algorithms.
Added registers 5, 6 and 7 “FPD West ADC sum low threshold”, “med” and “high”.

Object 5, Index 16, BW001:
Changed register names from “BEMC-high-tower-thX” to “BEMC-West high-tower-thX” to distinguish East from West.

Object 6, Index 16, BE001:
Changed register names from “BEMC-high-tower-thX” to “BEMC-East high-tower-thX” to distinguish East from West.

28th October 2004:

FIRST VERSION FOR 2005 RUNNING PERIOD

Added a comment at the beginning to say what these registers are.

Object 1, Index 25, VT201:
Added registers 8, 9 and 10 for “DeltaT Scalar Bit” selection. NOTE: These registers exist but are not actually used yet by the algorithm

Object 8, Index 24, BB005
This BBC large-tile DSM is now using the small-tile algorithms. The original 2 registers were replaced with the 4 registers used by the small-tile algorithms, but the names were changed to indicate this was a large-tile DSM, e.g. “BBC small-tile ADC threshold” became “BBC large-tile ADC threshold:, etc….

Object 8, Index 25, BB006
This new DSM is the second BBC large-tile DSM. It has the same algorithm and registers as Object 8, Index 24, BB005 (see above).

Object 9, Indices 16:22 (FE001:FE007) and 24:27 (FE008:FE011)
Three registers were added to all these DSMs for the FPD high-tower algorithms: “FPD East high-tower-th0”, “th1” and “th2”.

Object 10, Indices 16:22 (FE001:FE007) and 24:27 (FE008:FE011)
Three registers were added to all these DSMs for the FPD high-tower algorithms: “FPD West high-tower-th0”, “th1” and “th2”.

17th March 2006

FIRST VERSION FOR 2006 RUNNING PERIOD

Object 1, Index 23, LD301
Changed the meaning of registers 0-3 and removed register 4 for the 2006 algorithm.

Object 1, Index 26, EM201
Changed the meaning of registers 3 and 4 from jet-patch control to energy-sum control.

Object 1, Index 30, FP201
Added registers 8 and 9 and redefined the meaning of registers 3 to 9 for the new FPD++.

Object 2, Indices 33 and 16:22, BE/BW/EE10X
Added register 3 (TP-select) and register 4 (HT.TP-select)

Object 2, Indices 23:31 (EE001:EE009)
Added registers 3, 4 and 5 for the 3 TP thresholds

Object 5, Indices 16:30 (BW001:BW015)
Added registers 3, 4 and 5 for the 3 TP thresholds

Object 6, Indices 16:30 (BE001:BE015)
Added registers 3, 4 and 5 for the 3 TP thresholds

Object 8, Index 28 (MD001)
Added register 0 for the MTD ADC threshold

Object 9, Indices 16:27 (FE001:FE011)
All registers were removed. These registers were used temporarily while the PFD group tested the high tower algorithms which are no longer in use.

Object 10, Indices 16:27 (FW001:FW011)
All high tower registers were removed (see above)

Object 10, Indices 23 and 28 (FW101 and FW102)
Added register 0 for the module bitmask

21st March 2006
Object 9, Indices 23 and 28 (FE101 and FE102)
Added register 0 for the module bitmask